YMZ702D

Yamaha Piano Keyboard Scanning IC

1 Features

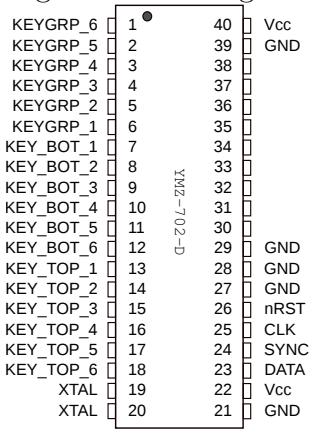
- Operates from single 5V supply and 4MHz oscillator.
- Simple digital output
- xxx mA current?
- Found in Yamaha Piano Keyboards (e.g. CLP 920)

2 Description

The YMZ-702-D is a piano keyboard scanning IC found inside some high end Yamaha piano keyboards. It connects velocity sensitive keyboard inputs to a simple digital output for consumption by an FPGA or micro-processor. This datasheet is based on the examination of one in a CLP-920. As there are no datasheets available for this part, this information may be useful to anyone wanting to interface to an old Yamaha keyboard perhaps for the purpose of MIDIfying it. The information contained in this unofficial datasheet has been obtained by visual inspection of the PCB and by monitoring the inputs / outputs of the device whilst in use in an original Yamaha Digital Piano. I do not warrant the accuracy of this information and any use of it is at your own risk.

3 Pins

Figure 1: Pin diagram



Pin	Symbol	Description
1	KEYGRP_6	Common connection for key group 6
2	KEYGRP_5	Common connection for key group 5
3	KEYGRP_4	Common connection for key group 4
4	KEYGRP_3	Common connection for key group 3
5	KEYGRP_2	Common connection for key group 2
6	KEYGRP_1	Common connection for key group 1
7	KEY_TOP_1	Top pad for key 1 in group
8	KEY_TOP_2	Top pad for key 2 in group
9	KEY_TOP_3	Top pad for key 3 in group
10	KEY_TOP_4	Top pad for key 4 in group
11	KEY_TOP_5	Top pad for key 5 in group
12	KEY_TOP_6	Top pad for key 6 in group
13	KEY_BOT_1	Bottom pad for key 1 in group
14	KEY_BOT_2	Bottom pad for key 2 in group
15	KEY_BOT_3	Bottom pad for key 3 in group
16	KEY_BOT_4	Bottom pad for key 4 in group
17	KEY_BOT_5	Bottom pad for key 5 in group
18	KEY_BOT_6	Bottom pad for key 6 in group
19	XTAL	4MHz oscillator connection. (Crystal?)
20	XTAL	4MHz oscillator connection.
21	GND	Ground
22	Vcc	Supply voltage. This is 5V and has a decoupling capacitor.
23	DATA	Data output
24	SYNC	Synchronisation input possibly initialisation too.
25	CLK	Clock output
26	nRST	Inverted reset. (Possibly? In operation it is driven at 5V and doesn't appear to change).
27	GND	Ground / Unknown. On the CLP-920 keyboard, these pins are connected to ground.
28	GND	
29	GND	
...		
39	GND	Ground
40	Vcc	Supply voltage. This is 5V and has a decoupling capacitor.

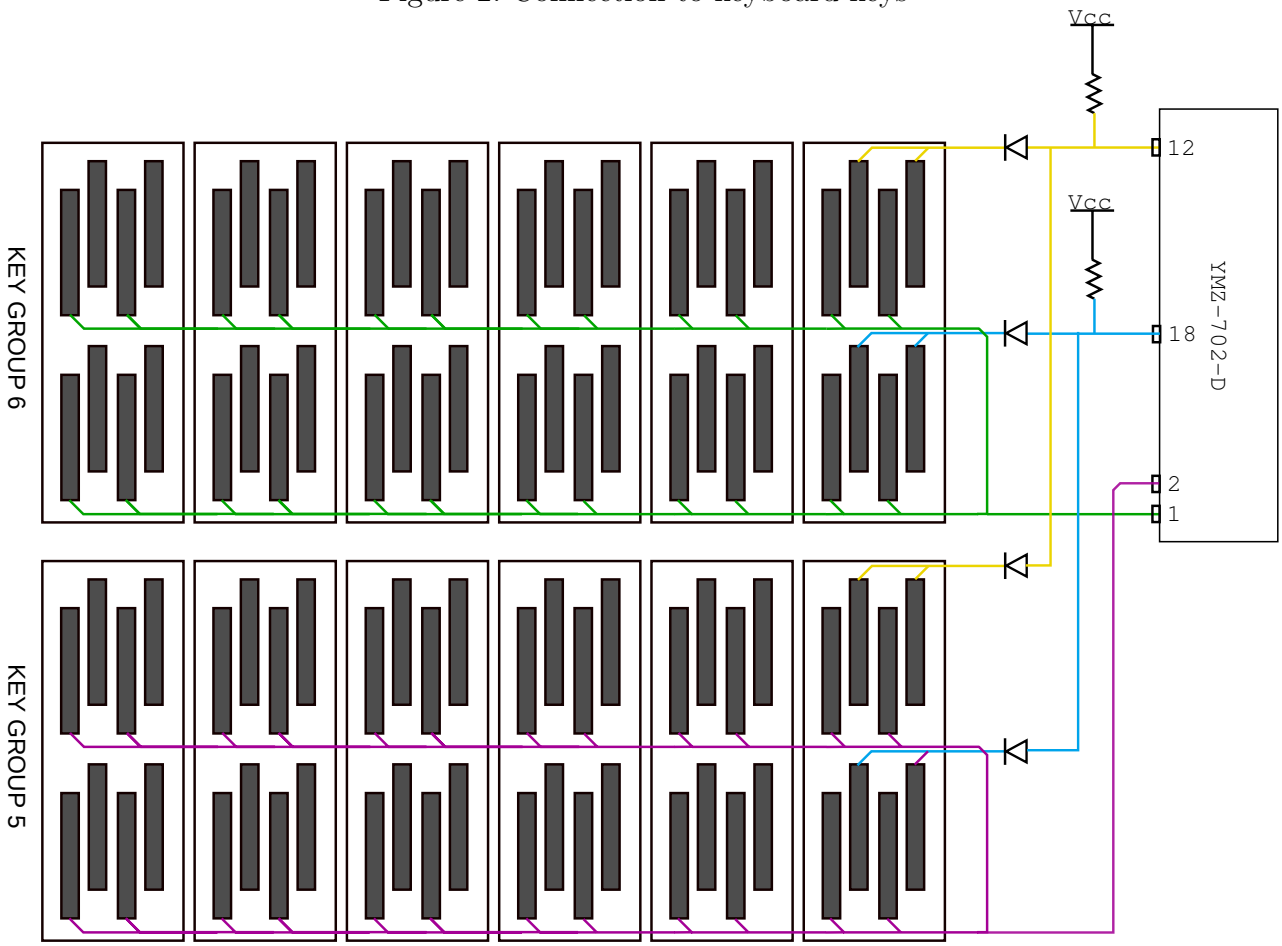
Table 1: Pin listing for YMZ702D

Unlisted pins 30-38 connect to the next PCB of the keyboard. They are presumably additional KEYGRP_x connections. Pins 7-18 need external pull-ups to Vcc.

4 Keyboard connections

It is assumed you have this device in a keyboard so these pins are not important for the purpose of interfacing to the digital side. As we are primarily interested in the digital connections this section is brief. For the curious who are looking for somewhere to probe the circuit looks to be approximately like this :

Figure 2: Connection to keyboard keys



Keys have two pads, top and bottom. Keys are divided into groups of six. Every key in the group is connected to its own KEYGRP_x pin.

For each group, The other side of the key is connected to KEY_BOT_x and KEY_TOP_x through a diode where x is the key number 1 to 6.

5 Device initialisation

Figure 3 shows a possible asynchronous (other digital IO lines seem to be quiet) initialisation from a CLP-920. When the CLP-920 is powered up, the SYNC channel (shown here on channel 1) is driven by the CLP-920 main PCB as follows :

It is unknown what this initialisation sequence does, if anything. The YMZ702D IC possibly replies with one byte of data after this sequence. I will confirm this if/when I get around to playing with it again.

6 Clock/Data output

The idle state of these lines is HI. Each byte (8-bits) is transferred at the request of the host. To request a byte, the SYNC line transitions HI LO HI. After this, a byte is transferred when it is ready. Data is only transferred when available so there may be some delay between the SYNC line request and the actual transfer taking place.

Data is transferred with a clock at 1MHz. Data is valid on the rising edge of CLK.

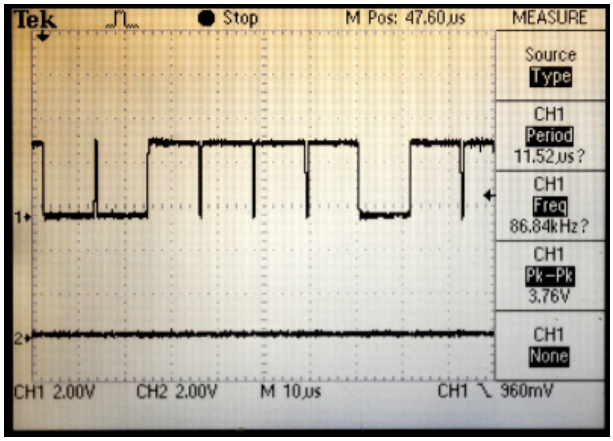


Figure 3: Device initialisation

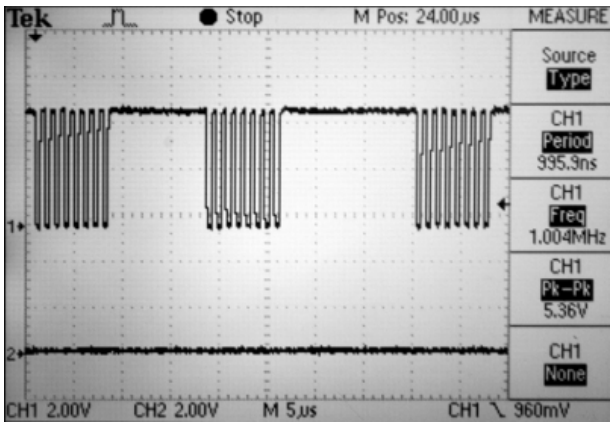


Figure 4: Clock trace

Each event (Key up, down, others?) results in 3 bytes of data. Crude observations indicate that:

- Byte 1 contains the key direction and other flags.
- Byte 2 contains the actual key pressed.
- Byte 3 contains the velocity (how hard the key was pressed / (released too?).